Version with Markings to Show Changes Made

TITLE OF THE INVENTION

SEMICONDUCTOR DEVICE ~~INCLUDING~~ WITH SCHOTTKY ELECTRODE ~~OF~~ INCLUDING LANTHANUM AND BORON, AND MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

(1) Field of the Invention

[0001] The present invention relates to a semiconductor device with a Schottky junction electrode made of a compound semiconductor and its manufacturing method.

(2) Description of the Related Art

[0002] In recent years, a Field Effect Transistor (hereinafter, referred to simply as FET), made of a compound semiconductor, for example, Ⅲ－Ⅴ family materials such as GaAs or InP, ~~is~~ has been widely employed for wireless communication and especially ~~for~~ as a power amplifier, a switch and the like of a cell phone terminal. Among FETs made of GaAs out of FETs made of ~~the~~ a compound semiconductor, a Pseudomorphic High Electron Mobility Transistor (hereinafter, referred to simply as PHEMT) is generally utilized. Here, PHEMT is a FET with good high-frequency wave ~~characteristic~~ characteristics including a strain channel layer generated by bonding two types of semiconductors whose lattice constants are a little different. The FETs made of GaAs, for example, include the strain channel layer generated by bonding InGaAs and AlGaAs.

[0003] In the GaAs PHEMT like this, however, an AlGaAs layer that is composed of AlGaAs has a Schottky contact with a gate electrode; parts of both sides in the portion of the AlGaAs layer that ~~does~~ do not touch the gate electrode are exposed by recess etching. As a result, a natural oxide film is formed on the surface of the AlGaAs layer, and its surface level density increases even if the AlGaAs layer is protected by a protective insulation film. Especially when the PHEMT is a power FET, the power FET does not work well because of frequency dispersion of current characteristic.

[0004] A prior art to solve the problem is "Manufacturing Method of Field Effect Transistor" (Japanese Laid-Open Patent application No. 09-045894 (pp. 3-4, Fig. 1)). The prior art resolves the problem by using an InGaP layer that is composed of InGaP that can better restrain the formation of the natural oxide film on the surface of a semiconductor layer than AlGaAs as the semiconductor layer that has the Schottky contact with the gate electrode.

[0005] Fig. 1 is a cross-sectional diagram of a conventional GaAs PHEMT.

[0006] In the GaAs PHEMT shown in Fig. 1, an epitaxial layer 120 is formed on a semi-insulating GaAs substrate 110 that is composed of semi-insulating GaAs. Here, the epitaxial layer 120 is made up of a GaAs buffer layer 121 that is composed of a 1-μm-thick ~~undope~~ undoped GaAs material and lessens a lattice mismatch between the epitaxial layer 120 and a semi-insulating GaAs substrate 110; an AlGaAs buffer layer 122 that is composed of an ~~undope~~ undoped AlGaAs material; a channel layer 123 that is composed of a 20-nm-thick ~~undope~~ undoped $In_{0.2}Ga_{0.8}As$ material and in which carriers run; a spacer layer 124 that is composed of a 5-nm-thick ~~undope~~ undoped InGaP material; a carrier supply layer 125 that is a planer-doped only one atom layer with Si, n-type impurity ions; a Schottky layer 126 that is composed of a 30-nm-thick ~~undope~~ undoped InGaP material; and an n^+-type GaAs cap layer 127 that is composed of a 100-nm-thick n^+-type GaAs.

[0007] Additionally, on the Schottky layer 126, a gate electrode 130 that has a Schottky contact with the Schottky layer 126 is formed; and at two parts on the n^+-type GaAs cap layer 127, two ohmic electrodes 140 are formed. Further, in the vicinity of the ohmic electrodes 140, two element separation regions 150 are formed; in the vicinity of the gate electrode 130, an insulation film 160 that is composed of SiN or SiO is formed.

[0008] As is described above, the conventional GaAs PHEMT can restrain an increase ~~of~~ in the surface level density because in the conventional GaAs PHEMT, a semiconductor layer that is composed of InGaP including In and P as constituents is used as the Schottky layer ~~126, and therefore~~ 126.

Therefore, the formation of a natural oxide film on the surface of the Schottky layer is restrained.

[0009] However, the conventional GaAs PHEMT has a problem explained below.

[0010] In the process of manufacturing the conventional GaAs PHEMT, since ~~the~~ heat of about 300 ℃ is added to the Schottky layer and the gate electrode, diffusion at the Schottky interface between the gate electrode and the Schottky layer occurs. As a result, a problem arises in that the Schottky characteristic deteriorates ~~arises~~. At this time, leak current of the Schottky junction between a Gate and a Source is larger than that of the conventional PHEMT having the Schottky layer that is composed of AlGaAs, and deterioration such as strain of a device is seen also in RF ~~characteristic~~ characteristics.

[0011] Fig. 2 is a diagram showing forward current-voltage ~~characteristic~~ characteristics between ~~the~~ a Gate and ~~the~~ a Source of the PHEMT that has ~~the~~ a Schottky layer that is composed of InGaP and the gate electrode that is composed of Ti. In Fig. 2, the broken line shows the forward current ~~the~~ voltage characteristic between the Gate and the Source of PHEMT before heat processing at ~~400℃~~ 400℃, while the solid line shows the forward current ~~the~~ voltage characteristic between the Gate and Source of PHEMT after the heat processing at 400℃.

[0012] It is apparent from Fig. 2 that the leak current at a time of low bias increases ~~by~~ due to the 400℃ heat processing and that the Schottky junction is greatly deteriorated.

SUMMARY OF THE INVENTION

[0013] In view of the foregoing, it is the object of the present invention to provide a semiconductor device and its manufacturing method. The semiconductor can restrain an increase ~~of~~ in the surface level density and has superior thermal stability. To achieve the above-mentioned object, the semiconductor of the present invention is a semiconductor device comprising: a Schottky layer; and a Schottky electrode that is formed on the

Schottky layer and has a Schottky contact with the Schottky ~~layer, wherein the~~ layer. The Schottky layer is composed of a compound semiconductor including In and P, and the portion of the Schottky electrode that touches the Schottky layer is composed of material whose main constituents are La and B. Here, it is acceptable that the Schottky layer is composed of one of InGaP, InP and ~~InAlGaP~~ InAlGaP, and that the portion of the Schottky electrode that touches the Schottky layer is composed of LaB_6. Additionally, it is agreeable that the semiconductor device is a transistor or a diode.

[0014] ~~Hereby, since~~ As noted above, the semiconductor device is made up of the Schottky layer that is composed of a compound semiconductor including In and P, and a Schottky electrode that is formed on the Schottky ~~layer~~ layer, and a portion of ~~which~~ the Schottky electrode that touches the Schottky layer is composed of ~~the~~ a material whose main constituents are La and ~~B, it has the effect of realizing~~ B. Therefore, the semiconductor device ~~that~~ can restrain an increase ~~of~~ in the surface level density of the Schottky ~~layer~~ layer, and has superior thermal stability and good Schottky ~~characteristic~~ characteristics.

[0015] Additionally, ~~it is possible that~~ the present invention ~~is~~ provides a method of manufacturing a semiconductor device that has (i) an epitaxial layer that comprises a semiconductor layer and a Schottky layer and (ii) a Schottky electrode that is formed on the Schottky layer and has a Schottky contact with the Schottky ~~layer, the~~ layer. The manufacturing method ~~including:~~ includes an epitaxial process of forming an epitaxial layer by forming in sequence a semiconductor layer and a Schottky layer that is composed of a compound semiconductor including In and P on a semi-insulating substrate by epitaxial growth using one of Metal Organic Chemical Vapor Deposition method and Molecular-Beam Epitaxial method; and an electrode forming process of forming a Schottky electrode by evaporating material whose main constituents are La and B onto the Schottky ~~layer, wherein~~ layer. In this process, the portion of the Schottky electrode that touches the Schottky layer is composed of the evaporated

material. Here, it is ~~passable~~ possible that the Schottky layer is composed of one of InGaP, InP and InAlGaP, and that the Schottky layer is formed in the epitaxial process, the Schottky layer being composed of one of InGaP, InP and InAlGap. Moreover, it is acceptable that the portion of the Schottky electrode that touches the Schottky layer is composed of LaB_6, and LaB_6 is evaporated onto the Schottky layer in the electrode forming process. Furthermore, it is agreeable that the vapor deposition of the material is performed with an electron-beam vapor deposition method.

[0016] Hereby, the Schottky electrode can be formed by vapor ~~deposition;~~ deposition, and it has the effect of ~~being able to~~ allowing manufacture of the semiconductor device with simple process.

[0017] As further information about technical background to this application, Japanese patent application No. 2003-031214 filed on February 7, 2003 is incorporated herein by reference.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] These and other subjects, advantages and features of the invention will become apparent from the following description thereof taken in conjunction with the accompanying drawings that illustrate a specific embodiment of the invention. ~~In the Drawings:~~

[0019] Fig. 1 is a cross-sectional diagram showing the structure of a conventional PHEMT.

[0020] Fig. 2 is a diagram showing forward current-voltage ~~characteristic~~ characteristics between a Gate and a Source of the conventional PHEMT.

[0021] Fig. 3 is a cross-sectional diagram showing the structure of a GaAs PHEMT according to the first embodiment of the present invention.

[0022] Fig. 4A~Fig. 4D are cross-sectional diagrams showing the structures of the GaAs PHEMTs indicating a manufacturing method for the GaAs PHEMT according to the first embodiment of the present invention.

[0023] Fig. 5 is a flowchart showing the method of manufacturing the GaAs PHEMT according to the first embodiment of the present invention.

[0024] Fig. 6 is a diagram showing forward current-voltage ~~characteristic~~

characteristics between a Gate and a Source of the GaAs PHEMT according to the first embodiment of the present invention.

[0025] Fig. 7 is a diagram showing forward current-voltage ~~characteristic~~ characteristics between the Gate and the Source of the GaAs PHEMT according to the first embodiment of the present invention and the conventional PHEMT.

[0026] Fig. 8 is a cross-sectional diagram showing the structure of an InP PHEMT according to the second embodiment of the present invention.

DESCRIPTION OF THE PREFERRED ~~EMBODIMENT(S)~~EMBODIMENT

[0027] The semiconductor device according to the present embodiments of the present invention will be explained below with reference to the figures.

(The First Embodiment)

[0028] Fig. 3 is a cross-sectional diagram showing the structure of a GaAs PHEMT according to the first embodiment.

[0029] In the PHEMT according to the first embodiment, an epitaxial layer 320 is formed on a semi-insulating GaAs substrate 310 that is composed of the semi-insulating GaAs material. Here, the epitaxial layer 320 is made up of a GaAs buffer layer 321 that is composed of a 1-μm-thick ~~undope~~ undoped GaAs material and lessens a lattice mismatch between the epitaxial layer 320 and the semi-insulating GaAs substrate 310; an AlGaAs buffer layer 322 that is composed of a 100-nm-thick ~~undope~~ undoped AlGaAs material; a channel layer 323 that is composed of a 20-nm-thick ~~undope~~ undoped $In_{0.2}Ga_{0.8}As$ material and in which carriers run; a spacer layer 324 that is composed of a 5-nm-thick ~~undope~~ undoped $Al_{0.25}Ga_{0.75}As$ material; a carrier supply layer 325 that is planer-doped only one atom layer with Si, n-type impurity ions so that the dose of Si is $5 \times 10^{12} cm^{-2}$; a spacer layer 326 that is composed of a 20-nm-thick ~~undope~~ undoped $Al_{0.25}Ga_{0.75}As$ material; a Schottky layer 327 that is composed of a 10-nm-thick ~~undope~~ undoped $In_{0.48}Ga_{0.52}P$ material; and an n^+-type GaAs cap layer 328 that is composed of a 100-nm-thick n^+-type GaAs material. By the way, the

Schottky layer 327 is described ~~to be~~ as being composed of $In_{0.48}Ga_{0.52}P$ material, but it may be composed of a compound semiconductor including In and P, for example, InGaP or InAlGaP.

[0030] Moreover, on the Schottky layer 327, a gate electrode 330 that has a Schottky contact with the Schottky layer 327 is ~~formed; at~~ formed. At two parts on the n^+-type GaAs cap layer 328, two ohmic electrodes 340 are formed. Further, in the vicinity of the ohmic electrodes 340, two element separation regions 350 are ~~formed; in~~ formed. In the vicinity of the gate electrode 330, an insulation film 360 that is composed of SiN or SiO is formed. Here, the gate electrode 330 is composed of material whose main constituents are La and B, for example, LaB_6.

[0031] Next, a manufacturing method of the GaAs PHEMT with the structure described above is explained following the cross-sectional diagram shown in Fig. 4 and the flowchart shown in Fig. 5. It should be noted that the same elements in Fig. 3 are given the same characters and their detailed explanations are omitted here.

[0032] For a start, as shown in Fig. 4A, on the semi-insulative GaAs substrate 310, using an MOCVD (metal organic chemical vapor deposition) method or MBE (molecular-beam epitaxial) method, epitaxial growth is performed in sequence to form the GaAs buffer layer 321, the AlGaAs buffer layer 322, the channel layer 323, the spacer layer 324, the carrier supply layer 325, the spacer layer 326, the Schottky layer 327 and the n^+-type GaAs cap layer 328 to form the epitaxial layer 320 (Step S510). Then, the element separation regions 350 are formed by shaping a pattern to form the element separation regions 350 with a photo resist 410 and doping the ions into the region where the element separation regions 350 are formed (Step S520). By the way, the element separation regions 350 may be formed by performing mesa etching to the regions where the element separation regions 350 in the epitaxial layer 320 are formed.

[0033] Next, as shown in Fig. 4B, an aperture is formed in the region where the ohmic electrodes 340 are formed by shaping a pattern to form the ohmic electrodes 340 with the photo resist and performing etching, and the ohmic

electrodes 340 are formed by evaporating an ohmic metal that is made of a Ni/Au/Ge alloy and lifting-off the photo resist (Step S530).

[0034] Now, as shown in Fig. 4C, an aperture is formed in the region where the gate electrode 330 ~~are~~ is formed by shaping a pattern to form the gate electrode 330 with the photo resist 420 and performing ~~etching; by~~ etching. By performing recess etching, the aperture is formed in the region where the gate electrode 330 between the ohmic electrodes 340 on the n^+-type GaAs cap layer 328 is ~~formed;~~ formed, and an aperture 430 is acquired (Step S540). At this time, since the etching selectivity between the n^+-type GaAs cap layer 328 and the Schottky layer 327 is large, a part of the n^+-type GaAs cap layer 328 can be selectively removed by the recess etching to form the aperture 430, using a liquid mixture of phosphoric acid, hydrogen peroxide solution and water, and therefore, it is possible to perform stable recess etching.

[0035] Next, as shown in Fig. 4D, the gate electrode 330 is formed by evaporating the gate metal that is composed of material whose main constituents are La and B, for example, LaB_6, using an electron-beam vapor deposition method and the like and lifting off the photo resist (Step S550).

[0036] Now, evaluation ~~result~~ results of the GaAs PHEMT according to the first embodiment ~~is~~ are shown.

[0037] Fig. 6 and Fig. 7 are diagrams showing the forward current-~~the~~ voltage characteristic between the Gate and the Source of the GaAs PHEMT according to the first embodiment. In Fig. 6, the dotted line shows the forward current-~~the~~ voltage characteristic between the Gate and the Source of the PHEMT having the gate electrode that is composed of LaB_6 before heat processing at 400℃; the solid line shows the forward current-~~the~~ voltage characteristic between the Gate and the Source of the PHEMT having the gate electrode that is composed of LaB_6 after ~~the~~ heat processing at 400℃. Additionally, in Fig. 7, the solid line shows the forward current-the voltage characteristic between the Gate and the Source of the PHEMT having the gate electrode that is composed of LaB_6 after ~~the~~ heat processing at 400℃; the broken line shows the forward current-~~the~~

voltage characteristic between the Gate and the Source of the PHEMT having the gate electrode that is composed of Ti after ~~the~~ heat processing at 400 ℃ ; and the dotted line shows the forward current ~~the~~ voltage characteristic between the Gate and the Source of the PHEMT having the gate electrode that is composed of Mo after ~~the~~ heat processing at 400℃.

[0038] ~~Seeing~~ In view of Fig. 6, it is apparent that the PHEMT having the gate electrode that is composed of LaB_6 according to the first embodiment is different from the conventional PHEMT having the gate electrode that is composed of ~~Ti,~~ Ti because its leak current does not increase after the heat processing at 400℃, and therefore, it has ~~the~~ a thermally stable Schottky characteristic.

[0039] Moreover, seeing Fig. 7, it is apparent that the PHEMT having ~~the~~ a gate electrode that is composed of LaB_6 has a higher Schottky barrier than the conventional PHEMT having ~~the~~ a gate electrode that is composed of Ti, and ~~that~~ the PHEMT having ~~the~~ a gate electrode that is composed of LaB_6 has a higher Schottky barrier than the PHEMT having ~~the~~ a gate electrode that is composed of ~~Mo, another~~ Mo (another high-melting point ~~metal~~ metal) by about ~~0.1V, and therefore, it~~ 0.1V. Therefore, the PHEMT has good Schottky ~~characteristic~~ characteristics.

[0040] As is described above, according to the first embodiment, the Schottky layer 327 is composed of $In_{0.48}Ga_{0.52}P$ material and the gate electrode 330 is composed of LaB_6 material, a high-melting point metal (melting point: 2806℃). Consequently, interdiffusion by heat processing between the Schottky layer 327 and the gate electrode 330 can be ~~restrained;~~ restrained, and it is possible to ~~realize the~~ obtain a PHEMT with superior thermal stability.

[0041] Furthermore, according to the first embodiment, the Schottky layer 327 is composed of $In_{0.48}Ga_{0.52}P$ material. Therefore, the PHEMT according to the first embodiment can ~~realize the PHEMT that can~~ restrain an increase of the surface level density of the Schottky layer.

[0042] Additionally, according to the first embodiment, the Schottky layer 327 is composed of $In_{0.48}Ga_{0.52}P$ material and the gate electrode 330 is

composed of LaB_6. Consequently, the PHEMT according to the first embodiment can realize the PHEMT with good Schottky ~~characteristic~~ characteristics.

[0043] Moreover, according to the first embodiment, the gate electrode 330 is formed by vapor deposition. Therefore, the PHEMT can be manufactured with a simple process.

[0044] By the way, according to the first embodiment, the PHEMT is exemplified as ~~the~~ a semiconductor device having (1) the gate electrode 330 that has a Schottky contact with the Schottky layer 327 and (2) the Schottky layer 327. But it is acceptable that the semiconductor device is another semiconductor device having (1) the gate electrode 330 that has a Schottky contact with the Schottky layer 327 and (2) the Schottky layer 327, for example, a Schottky diode.

[0045] Furthermore, according to the first embodiment, the gate electrode 330 is described to be composed of the material whose main constituents are La ~~and B~~ and B, but it is acceptable that the gate electrode is a lamination layer in which a layer that is composed of another material is formed on the layer that is composed of the material whose main constituents are La and B. At this time, in the process ~~to form~~ of forming the gate electrode 330, the lamination layer is formed by evaporating the gate metal that is composed of another material onto the gate electrode 330 after evaporating the gate metal that is composed of the material whose main constituents are La and B onto the gate electrode 330.

(The Second Embodiment)

[0046] Fig. 8 is a cross-sectional diagram showing the structure of an InP PHEMT according to the second embodiment of the present invention.

[0047] In the PHEMT according to the second embodiment, an epitaxial layer 820 is formed on a semi-insulating InP substrate 810 that is composed of the semi-insulating InP. Here, the epitaxial layer 820 is made up of an InAlAs buffer layer 821 that is composed of a 1-μm-thick ~~undope~~ undoped InAlAs material and lessens a lattice mismatch between the epitaxial layer

820 and the semi-insulating InP substrate 810; a channel layer 822 that is composed of a 20-nm-thick ~~undope~~ undoped $In_{0.53}Ga_{0.47}As$ material and in which carriers run; a spacer layer 823 that is composed of a 5-nm-thick ~~undope~~ undoped InAlGaAs material; a carrier supply layer 824 that is planer-doped only one atom layer with Si, n-type impurity ions so that the dose is $5 \times 10^{12}cm^{-2}$; an InAlAs layer 825 that is composed of a 20-nm-thick ~~undope~~ undoped InAlAs material; a Schottky layer 826 that is composed of a 10-nm-thick ~~undope~~ undoped InP material; and an n^+-type InGaAs cap layer 827 that is composed of a 100-nm-thick n^+-type InGaAs material. By the way, the Schottky layer 826 is described to be composed of InP but it may be composed of a compound semiconductor including In and P, for example, InAlGaP.

[0048] Additionally, on the Schottky layer 826, a gate electrode 830 that has a Schottky contact with the Schottky layer 826 is formed; and at two parts on the n^+-type InGaAs cap layer 827, two ohmic electrodes 840 are formed. Further, in the vicinity of the ohmic electrodes 840, two element separation regions 850 are ~~formed; in~~ formed. In the vicinity of the gate electrode 830, an insulation film 860 ~~is~~ composed of SiN or SiO is formed. Here, the gate electrode 830 is composed of material whose main constituents are La and B, for example, LaB_6.

[0049] Next, a manufacturing method of the InP PHEMT with the structure described above is explained. It should be noted that the figures are omitted because the InP PHEMT according to the second embodiment is manufactured by a method similar ~~method~~ to the manufacturing method of the GaAs PHEMT according to the first embodiment.

[0050] For a start, on the semi-insulative InP substrate 810, using an MOCVD method or an MBE method, epitaxial growth is performed in sequence to form the InAlAs buffer 821, the channel layer 822, the spacer layer 823, the carrier supply layer 824, the InAlAs layer 825, the Schottky layer 826, the n^+-type InGaAs cap layer ~~827 to~~ 827 which form the epitaxial layer 820. Then, the element separation regions 850 are formed by shaping a pattern to form the element separation regions 850 with a photo

resist and doping the ions into the region where the element separation regions 850 are formed.

[0051] Next, an aperture is formed in the region where the ohmic ~~electrode~~ electrodes 840 are formed by shaping a pattern to form the ohmic ~~electrode~~ electrodes 840 with the photo resist and performing ~~etching, and the~~ etching. The ohmic electrodes 840 are formed by evaporating an ohmic metal that is made of a Ni/Pt/Au alloy and lifting-off the photo resist.

[0052] Now, an aperture is formed in the region where the gate electrode 830 ~~are~~ is formed by shaping a pattern to form the gate electrode 830 with the photo resist and performing ~~etching; by~~ etching. By performing recess etching, the aperture is formed in the region where the gate electrode 830 between the ohmic electrodes 840 on the n^+-type InGaAs cap layer 827 is ~~formed;~~ formed, and an aperture is acquired. At this time, since the etching selectivity between the n^+-type InGaAs cap layer 827 and the Schottky layer 826 is large, a part of the n^+-type InGaAs cap layer 827 can be selectively removed by the recess etching to form the aperture, using a liquid mixture of phosphoric acid, hydrogen peroxide solution and ~~water, and therefore~~ water. Therefore, it is possible to perform stable recess etching.

[0053] Next, the gate electrode 830 is formed by evaporating the gate metal that is composed of material whose main constituents are La and B, for example, LaB_6, using the electron-beam vapor deposition method or the like and lifting off the photo resist.

[0054] As is described above, according to the second embodiment, the Schottky layer 826 is composed of InP and the gate electrode 830 is composed of LaB_6, a high-melting point metal. Consequently, interdiffusion by heat processing between the Schottky layer 826 and the gate electrode 830 can be ~~restrained;~~ restrained, and it is possible to realize the PHEMT with superior thermal stability.

[0055] Additionally, according to the second embodiment, the Schottky layer 826 is composed of InP and the gate electrode ~~330~~830 is composed of LaB_6. Therefore, the PHEMT according to the second embodiment can realize the PHEMT with good Schottky ~~characteristic~~ characteristics.

[0056] Moreover, according to the second embodiment, the Schottky layer 826 is composed of InP. Consequently, the PHEMT according to the second embodiment can realize the PHEMT that can restrain an increase of the surface level density of the Schottky layer.

[0057] Furthermore, according to the second embodiment, the gate electrode 830 is formed by vapor deposition. Therefore, the PHEMT can be manufactured with a simple process.

[0058] By the way, according to the second embodiment, the PHEMT is exemplified as the semiconductor device having (1) the gate electrode 830 that has a Schottky contact with the Schottky layer ~~826~~ 826, and (2) the Schottky layer 826. But it is acceptable that the semiconductor device is another semiconductor device having (1) the gate electrode 830 that has a Schottky contact with the Schottky layer ~~826~~ 826, and (2) the Schottky layer 826, for example, a Schottky diode.

[0059] Additionally, according to the second embodiment, the gate electrode 830 is described to be composed of ~~the~~ a material whose main constituents are La ~~and B~~ and B, but it is acceptable that the gate electrode is a lamination layer in which a layer that is composed of another material is formed on the layer that is composed of the material whose main constituents are La and B. At this time, in the process ~~to form~~ of forming the gate electrode 830, the lamination layer is formed by evaporating the gate metal that is composed of another material onto the gate electrode 830 after evaporating the gate metal that is composed of the material whose main constituents are La and B onto the gate electrode 830.

[0060] As is apparent from the above explanation, since the semiconductor device according to the present invention is made up of the Schottky layer that is composed of the compound semiconductor including In and P, and the Schottky electrode having a Schottky contact with the Schottky layer ~~and that is~~ composed of the material whose main constituents are La and B, it has the effect of realizing ~~the~~ a semiconductor device that is thermally stable and has good Schottky ~~characteristic~~ characteristics. Moreover, because the semiconductor device according to the present invention has

the Schottky layer that is composed of the compound semiconductor including In and P, it has the effect of realizing ~~the~~ a semiconductor device that can restrain an increase of the surface level density of the Schottky layer. Furthermore, since the Schottky electrode in the semiconductor device according to the present invention is formed by ~~the~~ vapor deposition, it ~~has the effect of being able to~~ enables manufacture the PHEMT with simple process.

[0061] Consequently, since the present invention can restrain the increase of the surface level density in the Schottky layer and can provide a semiconductor device with superior thermal stability and good Schottky ~~characteristic~~ characteristics, its practical value is extremely high.

ABSTRACT OF THE DISCLOSURE

A semiconductor device and its manufacturing method. The semiconductor device has a semi-insulating GaAs substrate 310, a GaAs buffer layer 321 that is formed on the semi-insulating GaAs substrate 310, AlGaAs buffer layer 322, a channel layer 323, a spacer layer ~~324.~~324, a carrier supply layer 325, a spacer layer 326, a Schottky layer 327 ~~that is~~ composed of an ~~undope~~ undoped $In_{0.48}Ga_{0.52}P$ material, and an n^+-type GaAs cap layer ~~328, a~~ 328. A gate electrode 330 ~~that~~ is formed on the Schottky layer 327, and is composed of LaB_6 and has a Schottky contact with the Schottky layer ~~327~~ 327, and ohmic electrodes 340 ~~that~~ are formed on the n^+-type GaAs cap layer 328.